Transcend
Exceeding Your Expectations

TS2GUSD-P3

2GB microSD Card + Reader P3

Description

Transcend microSD card series are non-volatile, which means no external power is required to retain the information stored on it. Besides, it is also a solid-state device that without moving parts to skip or break down. Based on original NAND flash chip, Transcend microSD can offer an incredible combination of fast data transfer, great flexibility, excellent security and incredibly small size.

Features

- ROHS compliant product.
- Operating Voltage: 2.7 ~ 3.6V
- Operating Temperature: -25 ~ 85°C
- Durability: 10,000 insertion/removal cycles
- Fully compatible with SD card spec. v1.1
- Comply with SD Association File System Specification
- Mechanical Write Protection Switch with microSD adapter
- SD Host allows MultiMediaCard upward compatibility
- Form Factor: 11mm x 15mm x 1mm

Placement

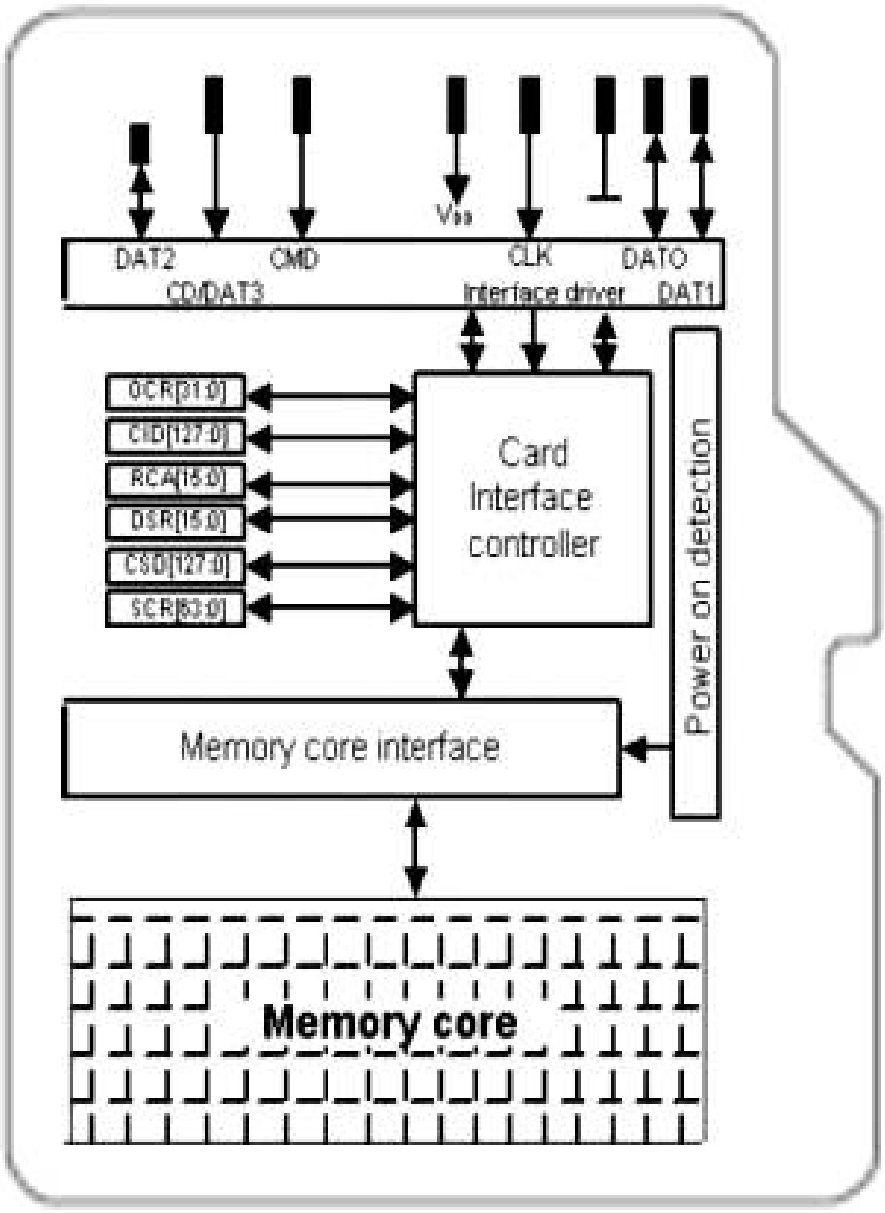
Front Back

Pin Definition

Pin No.	SD Mode			SPI Mode		
	Name	Type	Description	Name	Type	Description
1	DAT2	I/O/PP	Data Line [Bit2]	RSV		Reserved
2	CD/DAT3	I/O/PP	Card Detect / Data Line [Bit3]	CS	I	Chip Select
3	CMD	PP	Command / Response	DI	I	Data In
4	V_{DD}	S	Supply voltage	V_{DD}	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	V_{SS}	S	Supply voltage ground	V_{SS}	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit0]	DO	O/PP	Data out
8	DAT1	I/O/PP	Data Line [Bit1]	RSV		Reserved

S: Power Supply; I:Input; O:Output; PP:Push-Pull

Architecture



Bus Operating Conditions

• General

Parameter	Symbol	Min.	Max.	Unit	Remark
Peak voltage on all lines		-0.3	VDD+0.3	V	
All Inputs					
Input Leakage Current		-10	10	μA	
All Outputs					
Output Leakage Current		-10	10	μA	

• Power Supply Voltage

Parameter	Symbol	Min.	Max.	Unit	Remark
Supply voltage	V_{DD}	2.0	3.6	V	CMD0, 15,55,ACMD41 commands
Supply voltage specified in OCR register					Except CMD0, 15,55, ACMD41 commands
Supply voltage differentials (V_{SS1}, V_{SS2})		-0.3	0.3	V	
Power up time			250	ms	From 0v to V_{DD} Min.

Note. The current consumption of any card during the power-up procedure must not exceed 10 mA.

• Bus Signal Line Load

The total capacitance C_L the CLK line of the SD Memory Card bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself and the capacitance C_{CARD} of each card connected to this line:
$C_L = C_{HOST} + C_{BUS} + N*C_{CARD}$

Where N is the number of connected cards. Requiring the sum of the host and bus capacitances not to exceed 30 pF for up to 10 cards, and 40 pF for up to 30 cards, the following values must not be exceeded:

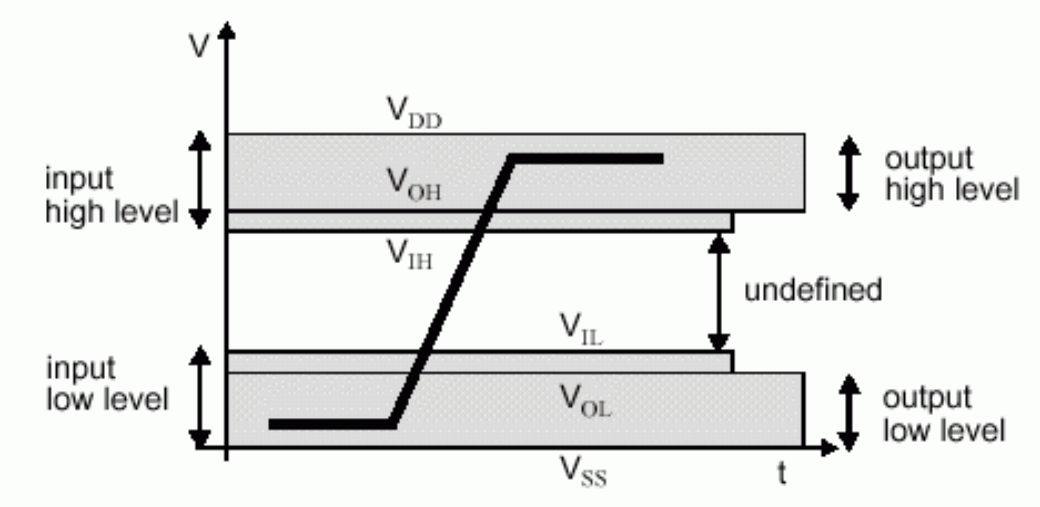
Parameter	Symbol	Min.	Max.	Unit	Remark
Bus signal line capacitance	C_L		100	pF	$f_{PP} \leq 20$ MHz, 7 cards
Single card capacitance	C_{CARD}		10	pF	
Maximum signal line inductance			16	nH	$f_{PP} \leq 20$ MHz
Pull-up resistance inside card (pin1)	R_{DAT3}	10	90	KΩ	May be used for card detection

Note that the total capacitance of CMD and DAT lines will be consist of C_{HOST}, C_{BUS} and one C_{CARD} only since they are connected separately to the SD Memory Card host.

Parameter	Symbol	Min.	Max.	Unit	Remark
Pull-up resistance	R_{CMD}, R_{DAT}	10	100	KΩ	To prevent bus floating
Bus signal line capacitance	C_L		250	pF	$f_{PP} \leq 5$ MHz, 21 cards

• Bus Signal Levels

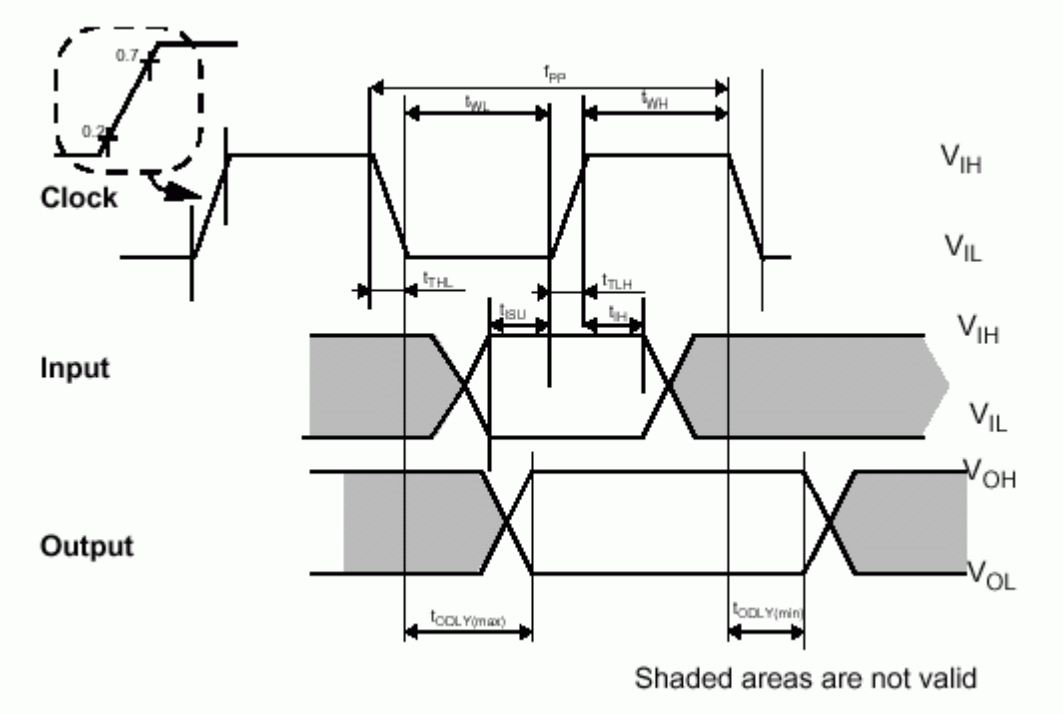
As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.



To meet the requirements of the JEDEC specification JESD8-1A, the card input and output voltages shall be within the following specified ranges for any V_{DD} of the allowed voltage range:

Parameter	Symbol	Min.	Max.	Unit	Remark
Output HIGH voltage	V_{OH}	0.75* V_{DD}		V	I_{OH} = -100 µA @V_{DD} min
Output LOW voltage	V_{OL}		0.125* V_{DD}	V	I_{OL} = 100 µA @V_{DD} min
Input HIGH voltage	V_{IH}	0.625* V_{DD}	V_{DD} + 0.3	V	
Input LOW voltage	V_{IL}	V_{SS} – 0.3	0.25* V_{DD}	V	

• Bus Timing



Parameter	Symbol	Min	Max.	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	25	MHz	$C_L \leq 100$ pF, (7 cards)
Clock frequency Identification Mode (The low freq. is required for MultiMediaCard compatibility.)	f_{OD}	0	400	KHz	$C_L \leq 250$ pF, (21 cards)
Clock low time	t_{WL}	10		ns	$C_L \leq 100$ pF, (7 cards)
		50		ns	$C_L \leq 250$ pF, (21 cards)
Clock high time	t_{WH}	10		ns	$C_L \leq 100$ pF, (7 cards)
		50		ns	$C_L \leq 250$ pF, (21 cards)
Clock rise time	t_{TLH}		10	ns	$C_L \leq 100$ pF, (7 cards)
			50	ns	$C_L \leq 250$ pF, (21 cards)
Clock fall time	t_{THL}		10	ns	$C_L \leq 100$ pF, (7 cards)
			50	ns	$C_L \leq 250$ pF, (21 cards)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5		ns	$C_L \leq 25$ pF, (1 cards)
Input hold time	t_{IH}	5		ns	$C_L \leq 25$ pF, (1 cards)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time	t_{ODLY}	0	14	ns	$C_L \leq 25$ pF, (1 cards)

Reliability and Durability

Temperature	Operation: -25°C / 85°C Storage: -40°C (168h) / 85°C (500h) Junction temperature: max. 95°C
Moisture and corrosion	Operation: 25°C / 95% rel. humidity Storage: 40°C / 93% rel. hum./500h Salt Water Spray: 3% NaCl/35C; 24h acc. MIL STD Method 1009
Durability	10000 mating cycles
Bending	10N
Torque	0.10N*m , +/- 2.5deg max
Drop test	1.5m free fall
UV light exposure	UV: 254nm, 15Ws/cm² according to ISO 7816-1
Visual inspection Shape and form	No warppage; no mold skin; complete form; no cavities surface smoothness <= -0.1 mm/cm² within contour; no cracks; no pollution (fat, oil dust, etc.)

Above technical information is based on standard data and tested to be reliable. However, Transcend makes no warranty, either expressed or implied, as to its accuracy and assumes no liability in connection with the use of this product. Transcend reserves the right to make changes in specifications at any time without prior notice.

Register Information

Within the card interface six registers are defined: OCR, CID, CSD, RCA, DSR and SCR. These can be accessed only by corresponding commands (see Chapter 4.7). The OCR, CID, CSD and SCR registers carry the card/content specific information, while the RCA and DSR registers are configuration registers storing actual configuration parameters.

1. OCR register

The 32-bit operation conditions register stores the V_{DD} voltage profile of the card. In addition, this register includes a status information bit. This status bit is set if the card power up procedure has been finished. The OCR register shall be implemented by the cards which do not support the full operating voltage range of the SD Memory Card bus, or if the card power up extends the definition in the timing diagram.

OCR bit position	VDD voltage window
0-3	reserved
4	reserved
5	reserved
6	reserved
7	reserved
8	2.0-2.1
9	2.1-2.2
10	2.2-2.3
11	2.3-2.4
12	2.4-2.5
13	2.5-2.6
14	2.6-2.7
15	2.7-2.8
16	2.8-2.9
17	2.9-3.0
18	3.0-3.1
19	3.1-3.2
20	3.2-3.3
21	3.3-3.4
22	3.4-3.5
23	3.5-3.6
24-30	reserved
31	card power up status bit (busy)1

A voltage range is not supported if the corresponding bit value is set to LOW. As long as the card is busy, the corresponding bit (31) is set to LOW.

2. CID Register

The Card IDentification (CID) register is 128 bits wide. It contains the card identification information used during the card identification phase. Every individual flash card shall have a unique identification number. The structure of the CID register is defined in the following paragraphs:

Name	Field	Width	CID-slice
Manufacturer ID	MID	8	[127:120]
OEM/Application ID	OID	16	[119:104]
Product name	PNM	40	[103:64]
Product revision	PRV	8	[63:56]
Product serial number	PSN	32	[55:24]
reserved	--	4	[23:20]
Manufacturing date	MDT	12	[19:8]
CRC7 checksum	CRC	7	[7:1]
not used, always '1'	-	1	[0:0]

• MID

An 8 bit binary number that identifies the card manufacturer. The MID number is controlled, defined and allocated to a SD Memory Card manufacturer by the SD Group. This procedure is established to ensure uniqueness of the CID register.

• OID

A 2 ASCII string characters that identifies the card OEM and/or the card contents (when used as a distribution media either on ROM or FLASH cards). The OID number is controlled, defined and allocated to a SD Memory Card manufacturer by the SD Group. This procedure is established to ensure uniqueness of the CID register.

• PNM

The product name is a string, 5 ASCII characters long.

• PRV

The product revision is composed of two Binary Coded Decimal (BCD) digits, four bits each, representing an "n.m" revision number. The "n" is the most significant nibble and "m" is the least significant nibble.
As an example, the PRV binary value field for product revision "6.2" will be: 0110 0010

• PSN

The Serial Number is 32 bits of binary number.

• MDT

The manufacturing date composed of two hexadecimal digits, one is 8 bit representing the year(y) and the other is four bits representing the month(m).
The “m” field [11:8] is the month code. 1 = January.
The “y” field [19:12] is the year code. 0 = 2000.
As an example, the binary value of the Date field for production date “April 2001” will be:
00000001 0100.

• CRC
CRC7 checksum (7 bits).

3. CSD Register

The Card-Specific Data register provides information on how to access the card contents. The CSD defines the data format, error correction type, maximum data access time, whether the DSR register can be used etc. The programmable part of the register (entries marked by W or E, see below) can be changed by CMD27. The type of the entries in the table below is coded as follows: R= readable, W(1) = writable once, W = multiple writable.

Name	Field	Width	Cell Type	CSD-slice
CSD structure	CSD_STRUCTURE	2	R	[127:126]
reserved	-	6	R	[125:120]
data read access-time-1	TAAC	8	R	[119:112]
data read access-time-2 in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]
max. data transfer rate	TRAN_SPEED	8	R	[103:96]
card command classes	CCC	12	R	[95:84]
max. read data block length	READ_BL_LEN	4	R	[83:80]
partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]
write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]
read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]
DSR implemented	DSR_IMP	1	R	[76:76]
reserved	-	2	R	[75:74]
device size	C_SIZE	12	R	[73:62]
max. read current @VDD min	VDD_R_CURR_MIN	3	R	[61:59]
max. read current @VDD max	VDD_R_CURR_MAX	3	R	[58:56]
max. write current @VDD min	VDD_W_CURR_MIN	3	R	[55:53]
max. write current @VDD max	VDD_W_CURR_MAX	3	R	[52:50]

Name	Field	Width	Cell Type	CSD-slice
device size multiplier	C_SIZE_MULT	3	R	[49:47]
erase single block enable	ERASE_BLK_EN	1	R	[46:46]
erase sector size	SECTOR_SIZE	7	R	[45:39]
write protect group size	WP_GRP_SIZE	7	R	[38:32]
write protect group enable	WP_GRP_ENABLE	1	R	[31:31]
reserved for MultiMediaCard compatibility		2	R	[30:29]
write speed factor	R2W_FACTOR	3	R	[28:26]
max. write data block length	WRITE_BL_LEN	4	R	[25:22]
partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]
reserved	-	5	R	[20:16]
File format group	FILE_FORMAT_GRP	1	R/W(1)	[15:15]
copy flag (OTP)	COPY	1	R/W(1)	[14:14]
permanent write protection	PERM_WRITE_PROTECT	1	R/W(1)	[13:13]
temporary write protection	TMP_WRITE_PROTECT	1	R/W	[12:12]
File format	FILE_FORMAT	2	R/W(1)	[11:10]
reserved		2	R/W	[9:8]
CRC	CRC	7	R/W	[7:1]
not used, always'1'	-	1	-	[0:0]

The following sections describe the CSD fields and the relevant data types. If not explicitly defined otherwise, all bit strings are interpreted as binary coded numbers starting with the left bit first.

• CSD_STRUCTURE

Version number of the related CSD structure.

CSD_STRUCTURE	CSD structure version	Valid for SD Memory Card Physical Specification Version
0	CSD version No. 1.0	Version 1.0-1.10
1-3	reserved	

• TAAC

Defines the asynchronous part of the data access time.

TAAC bit position	code
2:0	time unit 0=1ns, 1=10ns, 2=100ns, 3=1µs, 4=10µs, 5=100µs, 6=1ms, 7=10ms
6:3	time value 0=reserved, 1=1.0, 2=1.2, 3=1.3, 4=1.5, 5=2.0, 6=2.5, 7=3.0, 8=3.5, 9=4.0, A=4.5, B=5.0, C=5.5, D=6.0, E=7.0, F=8.0
7	reserved

• NSAC

Defines the worst case for the clock dependent factor of the data access time. The unit for NSAC is100 clock cycles. Therefore, the maximal value for the clock dependent part of the data access time is 25.5k clock cycles.

The total access time N_{AC} as expressed in the Table 34 is the sum of TAAC and NSAC. It has to be computed by the host for the actual clock rate. The read access time should be interpreted as a typical delay for the first data bit of a data block or stream.

• TRAN_SPEED

The following table defines the maximum data transfer rate per one data line - TRAN_SPEED:

TRAN_SPEED bit	code
2:0	transfer rate unit 0=100kbit/s, 1=1Mbit/s, 2=10Mbit/s, 3=100Mbit/s, 4... 7=reserved
6:3	time value 0=reserved, 1=1.0, 2=1.2, 3=1.3, 4=1.5, 5=2.0, 6=2.5, 7=3.0, 8=3.5, 9=4.0, A=4.5, B=5.0, C=5.5, D=6.0, E=7.0, F=8.0
7	reserved

Note that for current SD Memory Cards that field must be always 0_0110_010b (032h) which is equal to 25MHz - the mandatory maximum operating frequency of SD Memory Card.

In High-Speed mode, that field must be always 0_1011_010b (05Ah) which is equal to 50MHz. And when the timing mode returns to the default by CMD6 or CMD0 command, its value will be 032h.

• CCC

The SD Memory Card command set is divided into subsets (command classes). The card command class register CCC defines which command classes are supported by this card. A value of '1' in a CCC bit means that the corresponding

command class is supported.

CCC bit	Supported card command class
0	class 0
1	class 1
.....	
11	class 11

• READ_BL_LEN

The maximum read data block length is computed as $2^{READ_BL_LEN}$. The maximum block length might therefore be in the range 512...2048 bytes (see Chapter 4.11 for details). Note that in SD Memory Card the WRITE_BL_LEN is always equal to READ_BL_LEN

READ_BL_LEN	Block length	Remark
0-8	reserved	
9	2^9 = 512 Bytes	
.....		
11	2^{11} = 2048 Bytes	
12-15	reserved	

• READ_BL_PARTIAL (always = 1 in SD Memory Card)

Partial Block Read is always allowed in SD Memory Card. It means that smaller blocks can be used as well. The minimum block size will be one byte.

• WRITE_BLK_MISALIGN

Defines if the data block to be written by one command can be spread over more than one physical block of the memory device. The size of the memory block is defined in WRITE_BL_LEN.
WRITE_BLK_MISALIGN=0 signals that crossing physical block boundaries is invalid.
WRITE_BLK_MISALIGN=1 signals that crossing physical block boundaries is allowed.

• READ_BLK_MISALIGN

Defines if the data block to be read by one command can be spread over more than one physical block of the memory device. The size of the memory block is defined in READ_BL_LEN.
READ_BLK_MISALIGN=0 signals that crossing physical block boundaries is invalid.
READ_BLK_MISALIGN=1 signals that crossing physical block boundaries is allowed.

• DSR_IMP

Defines if the configurable driver stage is integrated on the card. If set, a driver stage register (DSR)must be implemented also.

DSR_IMP	DSR type
0	no DSR implemented
1	DSR implemented

• C_SIZE

This parameter is used to compute the user's data card capacity (not include the security protected area). The memory capacity of the card is computed from the entries C_SIZE, C_SIZE_MULT and READ_BL_LEN as follows:

memory capacity = BLOCKNR * BLOCK_LEN

where

BLOCKNR = (C_SIZE+1) * MULT

MULT = $2^{C_SIZE_MULT+2}$ (C_SIZE_MULT < 8)

BLOCK_LEN = $2^{READ_BL_LEN}$, (READ_BL_LEN < 12)

Maximum capacity of the card, compliant to SD Physical Specification Versoin1.01 shall be up to2G bytes (2_{31} bytes) to be consistent with the maximum capacity (2G bytes) of SD Memory Card File System Specification Ver.1.01.
To indicate 2GByte card, BLOCK_LEN shall be 1024 bytes.
Therefore, the maximal capacity which can be coded is 4096*512*1024 = 2G bytes.
Example: A 32Mbyte card with BLOCK_LEN = 512 can be coded by C_SIZE_MULT = 3 and C_SIZE = 2000.

• VDD_R_CURR_MIN, VDD_W_CURR_MIN

The maximum values for read and write currents at the minimal power supply V_{DD} are coded as follows:

VDD_R_CURR_MIN VDD_W_CURR_MIN	code for current consumption @ V_{DD}
2:0	0=0.5mA; 1=1mA; 2=5mA; 3=10mA; 4=25mA; 5=35mA; 6=60mA; 7=100mA

• VDD_R_CURR_MAX, VDD_W_CURR_MAX

The maximum values for read and write currents at the maximal power supply V_{DD} are coded as follows:

VDD_R_CURR_MAX VDD_W_CURR_MAX	code for current consumption @ V_{DD}
2:0	0=1mA; 1=5mA; 2=10mA; 3=25mA; 4=35mA; 5=45mA; 6=80mA; 7=200mA

• C_SIZE_MULT

This parameter is used for coding a factor MULT for computing the total device size (see 'C_SIZE').

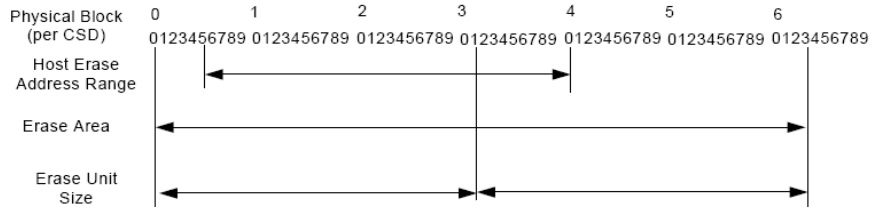
The factor MULT is defined as $2^{C_SIZE_MULT+2}$.

C_SIZE_MULT	MULT	Remark
0	$2^2 = 4$	
1	$2^3 = 8$	
2	$2^4 = 16$	
3	$2^5 = 32$	
4	$2^6 = 64$	
5	$2^7 = 128$	
6	$2^8 = 256$	
7	$2^9 = 512$	

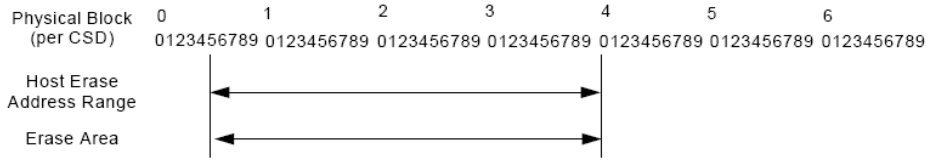
• ERASE_BLK_EN

The ERASE_BLK_EN defines the granularity of the unit size of the data to be erased. The erase operation can erase either one or multiple units of WRITE_BL_LEN or one or multiple units (orsectors) of SECTOR_SIZE (see definition below).

If ERASE_BLK_EN = ’0’, the host can erase one or multiple units of SECTOR_SIZE. The erase will start from the beginning of the sector that contains the start address to the end of the sector that contains the end address. For example, if SECTOR_SIZE=31 and the host sets the Erase Start Address to 5 and the Erase End Address to 40.



If ERASE_BLK_EN = ’1’ the host can erase one or multiple units of 512 bytes. All blocks that contain data from start address to end address are erased. For example, if the host sets the Erase Start Address to 5 and the Erase End Address to 40.



• SECTOR_SIZE

The size of an erasable sector. The contents of this register is a 7 bit binary coded value, defining the number of write

blocks (see WRITE_BL_LEN). The actual size is computed by increasing this number by one. A value of zero means 1 write block, 127 means 128 write blocks.

• WP_GRP_SIZE

The size of a write protected group. The contents of this register is a 7 bit binary coded value, defining the number of erase sectors (see SECTOR_SIZE). The actual size is computed by increasing this number by one. A value of zero means 1 erase sector, 127 means 128 erase sectors.

• WP_GRP_ENABLE

A value of '0' means no group write protection possible.

• R2W_FACTOR

Defines the typical block program time as a multiple of the read access time. The following table defines the field format.

R2W_FACTOR	Multiples of read access time
0	1
1	2 (write half as fast as read)
2	4
3	8
4	16
5	32
6,7	reserved

• WRITE_BL_LEN

The maximum write data block length is computed as $2^{WRITE_BL_LEN}$. The maximum block lengthmight therefore be in the range from 512 up to 2048 bytes. Write Block Length of 512 bytes isalways supported.
Note that in SD Memory Card the WRITE_BL_LEN is always equal to READ_BL_LEN.

WRITE_BL_LEN	Block length	Remark
0-8	reserved	
9	2^9 = 512 bytes	
.....		

WRITE_BL_LEN	Block length	Remark
11	2^{11} = 2048 Bytes	
12-15	reserved	

• WRITE_BL_PARTIAL

Defines whether partial block sizes can be used in block write commands.WRITE_BL_PARTIAL='0' means that only the WRITE_BL_LEN block size and its partial derivatives,in resolution of units of 512 bytes, can be used for block oriented data write.WRITE_BL_PARTIAL='1' means that smaller blocks can be used as well. The minimum block sizeis one byte.

• FILE_FORMAT_GRP

Indicates the selected group of file formats. This field is read-only for ROM.

• COPY

Defines if the contents is original (= '0') or has been copied (='1'). The COPY bit for OTP and MTPdevices, sold to end consumers, is set to '1' which identifies the card contents as a copy. The COPY bit is an one time programmable bit.

• PERM_WRITE_PROTECT

Permanently protects the whole card content against overwriting or erasing (all write and erase commands for this card are permanently disabled). The default value is '0', i.e. not permanently write protected.

• TMP_WRITE_PROTECT

Temporarily protects the whole card content from being overwritten or erased (all write and erase commands for this card are temporarily disabled). This bit can be set and reset. The default value is '0', i.e. not write protected.

• FILE_FORMAT

Indicates the file format on the card. This field is read-only for ROM. The following formats are defined:

FILE_ FORMAT_ GRP	FILE_FORMAT	Type
0	0	Hard disk-like file system with partition table
0	1	DOS FAT (floppy-like) with boot sector only (no partition table)
0	2	Universal File Format
0	3	Others / Unknown
1	0, 1, 2, 3	Reserved

• CRC

The CRC field carries the check sum for the CSD contents.
The checksum has to be recalculated by the host for any CSD modification. The default corresponds to the initial CSD contents.

The following table lists the correspondence between the CSD entries and the command classes. A '+' entry indicates that the CSD field affects the commands of the related command class.

	Command classes							
CSD Field	**0**	**2**	**4**	**5**	**6**	**7**	**8**	**9**
CSD_STRUCTURE	+	+	+	+	+	+	+	+
TAAC		+	+	+	+	+	+	
NSAC		+	+	+	+	+	+	
TRAN_SPEED		+	+					
CCC	+	+	+	+	+	+	+	+

	Command classes							
CSD Field	0	2	4	5	6	7	8	9
READ_BL_LEN		+						
WRITE_BLK_MISALIGN			+					
READ_BLK_MISALIGN		+						
DSR_IMP	+	+	+	+	+	+	+	+
C_SIZE_MANT		+	+	+	+	+	+	
C_SIZE_EXP		+	+	+	+	+	+	
VDD_R_CURR_MIN		+						
VDD_R_CURR_MAX		+						
VDD_W_CURR_MIN			+	+	+	+	+	
VDD_W_CURR_MAX			+	+	+	+	+	
ERASE_BLK_EN				+	+	+	+	
SECTOR_SIZE				+	+	+	+	
WP_GRP_SIZE					+	+	+	
WP_GRP_ENABLE					+	+	+	
R2W_FACTOR			+	+	+	+	+	
WRITE_BL_LEN			+	+	+	+	+	
WRITE_BL_PARTIAL			+	+	+	+	+	
FILE_FORMAT_GRP								
COPY	+	+	+	+	+	+	+	
PERM_WRITE_PROTECT	+	+	+	+	+	+	+	
TMP_WRITE_PROTECT	+	+	+	+	+	+	+	
FILE_FORMAT								
CRC	+	+	+	+	+	+	+	+

4. RCA Register

The writable 16-bit relative card address register carries the card address that is published by the card during the card identification. This address is used for the addressed host-card communication after the card identification procedure. The default value of the RCA register is 0x0000. The value0x0000 is reserved to set all cards into the *Stand-by State* with CMD7.

5. DSR Register (Optional)

The 16-bit driver stage register is described in detail in Chapter 6.5. It can be optionally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate or number of

cards). The CSD register carries the information about the DSR register usage. The default value of the DSR register is 0x404.

6. SCR Register

In addition to the CSD register there is another configuration register that named - SD CARD Configuration Register (SCR). SCR provides information on SD Memory Card's special features that were configured into the given card. The size of SCR register is 64 bit. This register shall be set in the factory by the SD Memory Card manufacturer.
The following table describes the SCR register content.

Description	Field	Width	Cell Type	SCR Slice
SCR Structure	SCR_STRUCTURE	4	R	[63:60]
SD Memory Card - Spec. Version	SD_SPEC	4	R	[59:56]
data_status_after erases	DATA_STAT_AFTER_ERASE	1	R	[55:55]
SD Security Support	SD_SECURITY	3	R	[54:52]
DAT Bus widths supported	SD_BUS_WIDTHS	4	R	[51:48]
reserved	-	16	R	[47:32]
reserved for manufacturer usage	-	32	R	[31:0]

• SCR_STRUCTURE

Version number of the related SCR structure in the SD Memory Card Physical Layer Specification.

SCR_STRUCTURE	SCR structure version	Valid for SD Physical Layer Specification Version
0	SCR version No. 1.0	Version 1.0-1.10
1-15	reserved	

• SD_SPEC

Describes the SD Memory Card Physical Layer Specification version supported by this card.

SD_SPEC	Physical Layer Specification Version Number
0	Version 1.0-1.01
1	Version 1.10
2-15	reserved

• DATA_STAT_AFTER_ERASE

Defines the data status after erase, whether it is '0' or '1' (the status is card vendor dependent).

• SD_SECURITY

Describes the security algorithm supported by the card.

SD_SECURITY	Supported algorithm
0	no security
1	security protocol 1.0
2	security protocol 2.0
3 .. 7	reserved

Security Protocol 1.0 relates to Security Specification Version 0.96.
Security Protocol 2.0 relates to Security Specification Version 1.0.-1.01
Note that it is mandatory for a regular writable SD Memory Card to support Security Protocol. For ROM (Read Only) and OTP (One Time Programmable) type of SD Memory Card the security feature is optional

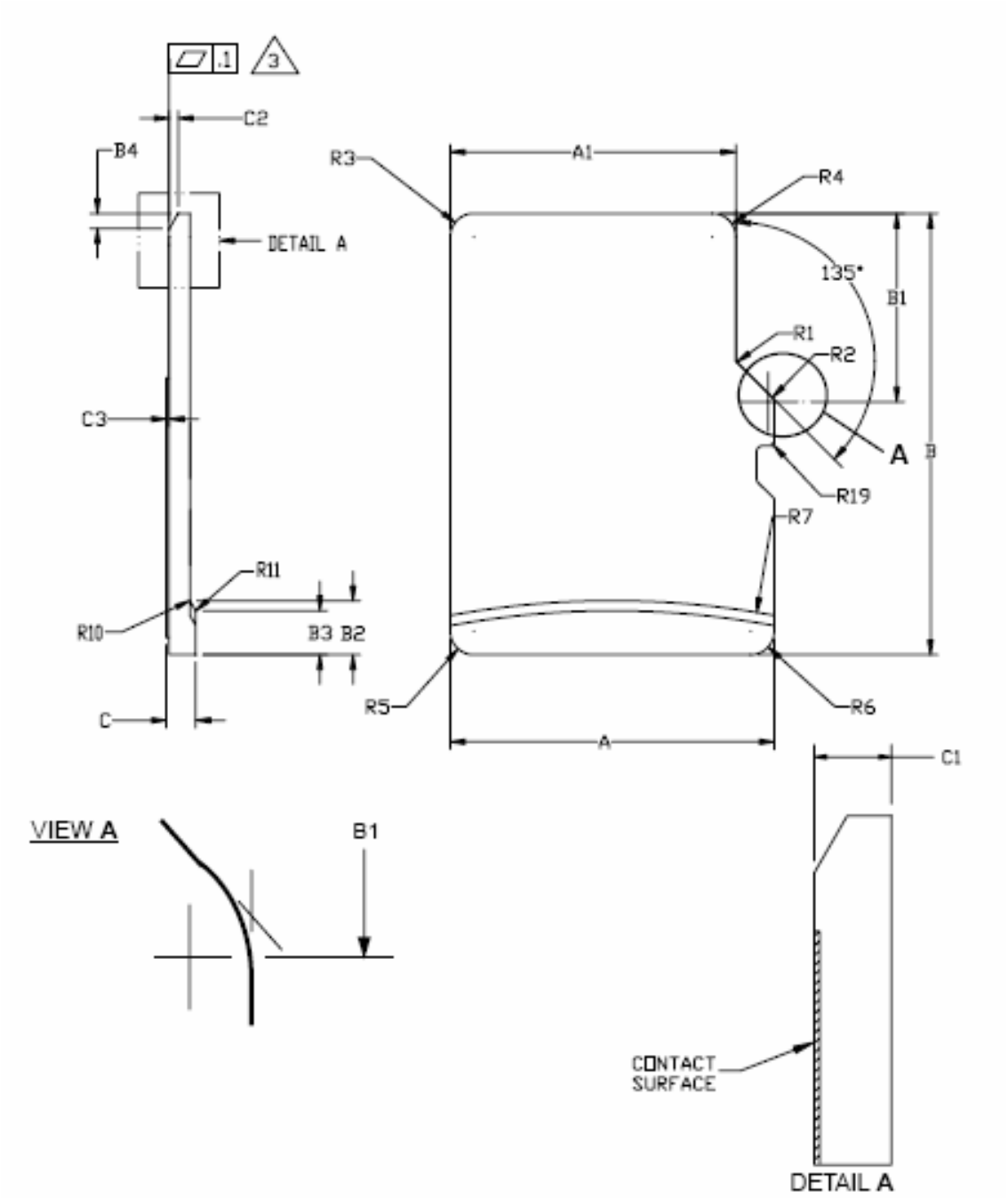
• SD_BUS_WIDTHS

Describes all the DAT bus widths that are supported by this card.

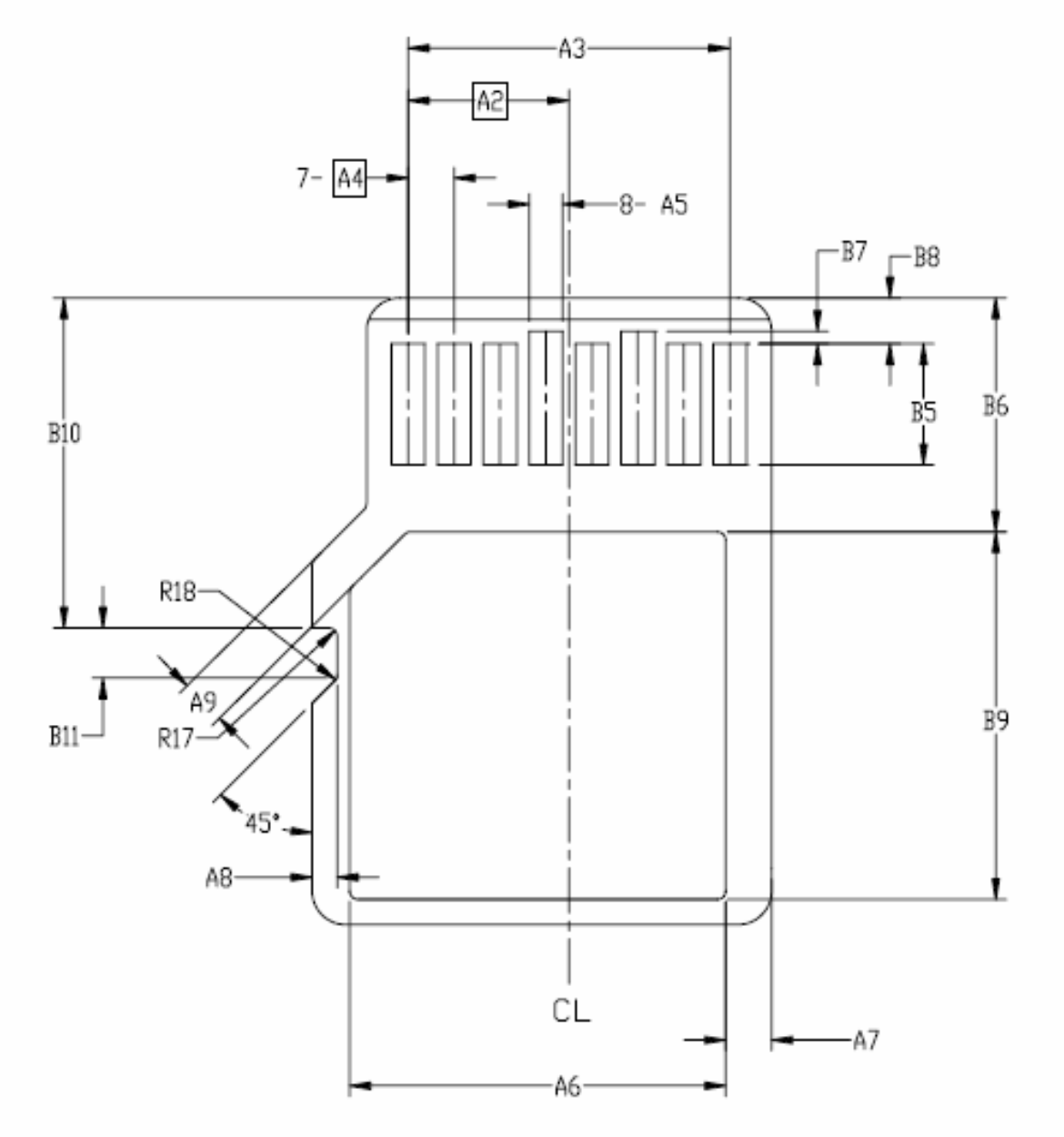
SD_BUS_WIDTHS	Supported Bus Widths
Bit 0	1 bit (DAT0)
Bit 1	reserved
Bit 2	4 bit (DAT0-3)
Bit 3 [MSB]	reserved

Since SD Memory Card shall support at least the two bus modes 1bit or 4bit width then any SD Card shall set at least bits 0 and 2 (SD_BUS_WIDTH="0101").

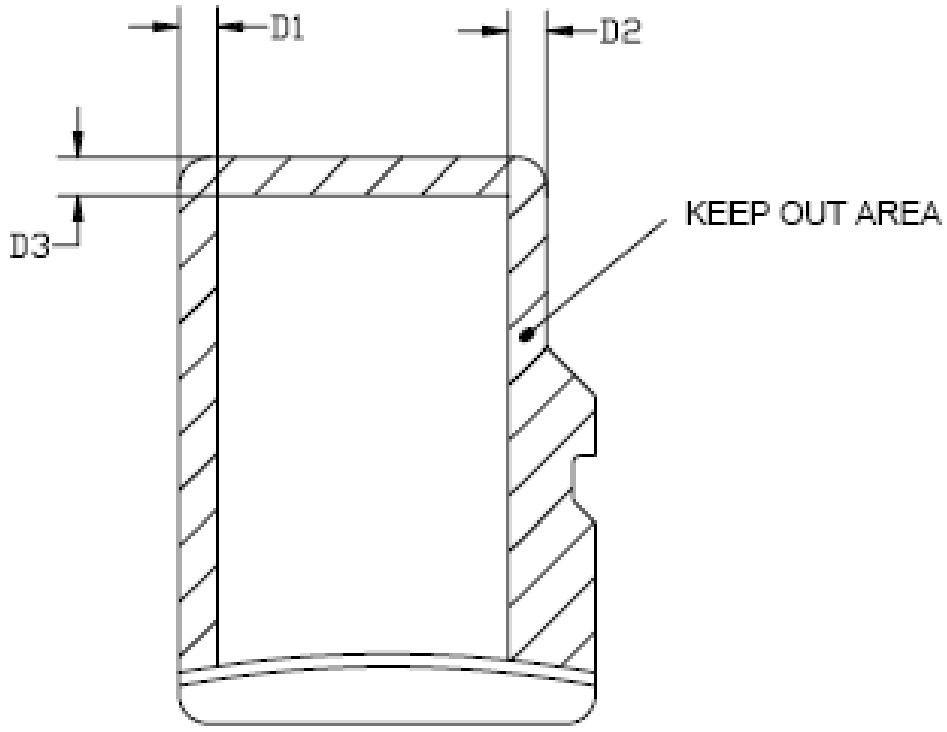
Mechanical Dimension



Mechanical Description: Top View



Mechanical Description: Bottom View



Mechanical Description: Keep Out Area

	COMMON DIMENSIONS			
SYMBOL	MIN	NOM	MAX	NOTE
A	10.90	11.00	11.10	
A1	9.60	9.70	9.80	
A2	-	3.85	-	BASIC
A3	7.60	7.70	7.80	
A4	-	1.10	-	BASIC
A5	0.75	0.80	0.85	
A6	-	-	8.50	
A7	0.90	-	-	
A8	0.60	0.70	0.80	
A9	0.80	-	-	
B	14.90	15.00	15.10	
B1	6.30	6.40	6.50	
B2	1.64	1.84	2.04	
B3	1.30	1.50	1.70	
B4	0.42	0.52	0.62	
B5	2.80	2.90	3.00	
B6	5.50	-	-	
B7	0.20	0.30	0.40	
B8	1.00	1.10	1.20	
B9	-	-	9.00	
B10	7.80	7.90	8.00	
B11	1.10	1.20	1.30	
C	0.90	1.00	1.10	
C1	0.60	0.70	0.80	
C2	0.20	0.30	0.40	
C3	0.00	-	0.15	
D1	1.00	-	-	
D2	1.00	-	-	
D3	1.00	-	-	
R1	0.20	0.40	0.60	
R2	0.20	0.40	0.60	
R3	0.70	0.80	0.90	
R4	0.70	0.80	0.90	
R5	0.70	0.80	0.90	
R6	0.70	0.80	0.90	
R7	29.50	30.00	30.50	
R10	-	0.20	-	
R11	-	0.20	-	
R17	0.10	0.20	0.30	
R18	0.20	0.40	0.60	
R19	0.05	-	0.20	

Notes:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

2. DIMENSIONS ARE IN MILLIMETERS.

3. COPLANARITY IS ADDITIVE TO C1 MAX THICKNESS.

microSD package: Dimensions

TS2GUSD-P3

2GB microSD Card + Reader P3

Description

RDP3 is a USB2.0 Compact Card Reader. It is designed for fast, easy data transfer and exchange using microSD Memory Card.

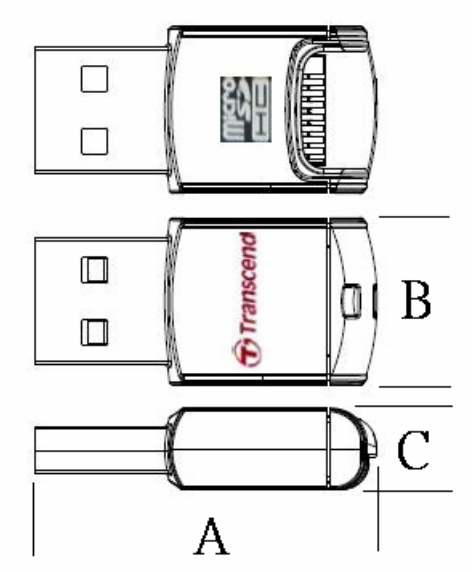
Features

- Fully Compliant with the Hi-Speed USB 2.0 specification
- USB powered (no external power or battery needed)
- Support the microSD Memory Card insertion directly

System Requirements

- Desktop or notebook computer with a working USB port
- One of the following Operating Systems:
  - Windows® Me
  - Windows® 2000
  - Windows® XP
  - Windows Vista™
  - Mac™ OS 9.0, or later
  - Linux™ Kernel 2.4, or later

Placement



Dimensions

Side	Millimeters	Inches
A	32.80 ± 1.0	1.29 ± 0.04
B	16.00 ± 1.0	0.63 ± 0.04
C	7.80 ± 1.0	0.31 ± 0.04

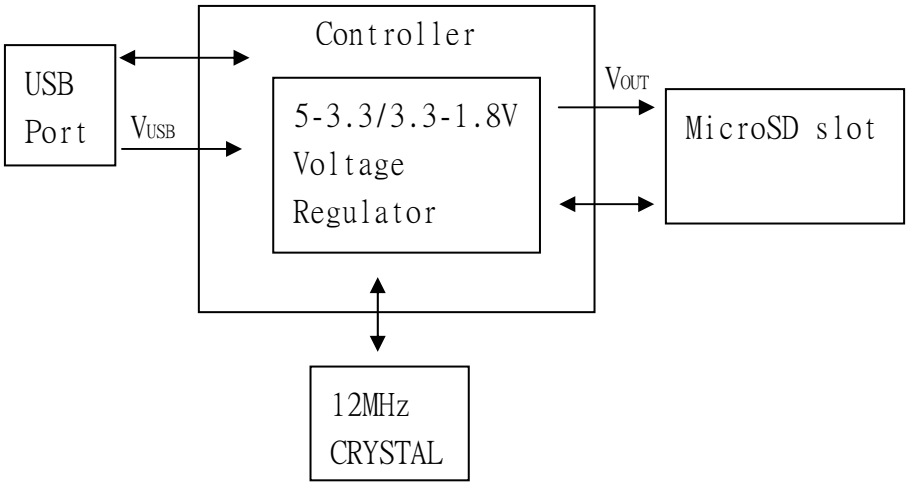
USB Pinouts

Pin No.	Pin Name
01	V_{USB}
02	D-
03	D+
04	VSS

USB Pin Identification

Symbol	Function
D- D+	USB differential signal: The pairs are used to transmit Data/Address/Command
VSS	Ground
V_{USB}	USB Power Input

Block Diagram



Recommended Operating Conditions:

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
V_{USB}	Power Supply	4.5	5.0	5.5	V
T_{OPR}	Operating Temperature	0		70	^{O}C

DC Characteristics:

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
V_{DD33}	Input Voltage	3.0	3.3	3.6	V
V_{DD18}	Input Voltage	1.62	1.8	1.98	V
V_{OUT}	Output Voltage	3.0	3.3	3.6	V

DC Electrical Characteristics of 3.3V I/O:

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
V_{IL}	Input Low Voltage	0		0.8	V
V_{IH}	Input High Voltage	2.0		3.6	V
V_{OL}	Output Low Voltage			0.4	V
V_{OH}	Output High Voltage	2.4			V

Above technical information is based on industry standard data and tested to be reliable. However, Transcend makes no warranty, either expressed or implied, as to its accuracy and assumes no liability in connection with the use of this product. Transcend reserves the right to make changes in specifications at any time without prior notice.